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Dual-Core Update to the Intel® Itanium® 2 Processor Reference Manual

For Software Development and Optimization

Revision 0.9

January 2006

Document Number: 308065-001

The Dual-Core Itanium 2 Processor   **intel**®

Specifically, the queue allocation policy now supports recovery of empty entries. This allows for greater availability of the L2 OzQ in light of accesses completed out of order.

The L2D also considers the thread identifier when performing ordering such that an ordered request from one thread is not needlessly ordered against another thread's accesses.

2.3.3.3   L3 Cache

Montecito's L3 cache remains unified as in previous Itanium 2 processors, but is now 12 MB. Even so, it maintains the same 14-cycle integer-access best case latency in the 6M and 9M Itanium 2 processors. Montecito's L3 cache uses an asynchronous interface with the data array to achieve this low latency; there is no clock, only a read or write valid indication. Four cycles after a read signal, index, and way, the entire 128-byte line is available and latched. The array then delivers this data in four cycles to either the L2D or L2I in critical-byte order.

Montecito's L3 receives requests from both the L2I and L2D but gives priority to the L2I request in the rare case of a conflict. Conflicts are rare because Montecito moves the arbitration point from the Itanium 2 processor L1-L2 to L2-L3. This greatly reduces conflicts because of L2I and L2D's high hit rates. The I and D arbitration point also reduces conflict and access pressure within the core; L1I misses go directly to the L2I and not through the core. L2I misses contend against L2D request for L3 access.

2.3.3.4   Request Tracking

All L2I and L2D requests are allocated to one of 16 request buffers. Requests are sent to the to the L3 cache and system from these buffers by the tracking logic. A modified L2D victim or partial write may be allocated to one of 8 write buffers. This is an increase of 2 over the Itanium 2 processor. The lifetime of the L2D victim buffers is also significantly decreased to further reduce pressure on them. Lastly, the L3 dirty victim resources has grown by 2 entries to 8 in Montecito.

In terms of write coalescing buffers (WCB), Montecito has 4 128B line WCBs in each core. These are fully shared between threads.

2.4   Threading

The multiple thread concept starts with the idea that the processor has some resources that cannot be effectively utilized by a single thread. Therefore, sharing under-utilized resources between multiple threads will increase utilization and performance. The Montecito processor Hyper-Threading Technology implementation duplicates and shares resources to create two logical processors. All architectural state and some micro-architectural state is duplicated.

The duplicated architectural state (general, floating point, predicate, branch, application, translation, performance monitoring, bank, and interrupt registers) allows each thread to appear as a complete processor to the operating system thus minimizing the changes needed at the OS level. The duplicated micro-architectural state of the return stack buffer and the advanced load address table (ALAT) prevent cross-thread pollution that would occur if these resources were shared between the two logical processors.

The two logical processors share the parallel execution resources (core) and the memory hierarchy (caches and TLBs). There are many approaches to sharing resources that vary from fixed time intervals, temporal multi-threading or TMT, to sharing resources concurrently, simultaneous multi-threading or SMT. The Montecito Hyper-Threading Technology approach blends both approaches such that the cores share threads using a TMT approach while the memory hierarchy shares resources using a SMT approach. The core TMT approach is further augmented with control

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January 23, 2006

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VIA FEDERAL EXPRESS

Barry W. Graham, Esq.
Finnegan, Henderson, Farabow, Garrett &
    Dunner, LLP
901 New York Avenue, NW
Washington, DC 20001-4413

. Re: *BLAX Corporation v. Intel Corporation and Analog Devices, Inc.*

Dear Mr. Graham

Please find enclosed five (5) disks which contain Intel Corporation production documents. The
disks contain documents Bates numbered as follows:

Disk 1	75004DOC000001 - 75004DOC000078
	75005DOC000001 - 75005DOC000054
	75006DOC000001 - 75006DOC005035
	75007DOC000001 - 75007DOC001190
	75008DOC000001 - 75008DOC000696
	75009DOC000001 - 75009DOC019683
	75010DOC000001 - 75010DOC000277
	75011DOC000001 - 75011DOC001142
	75012DOC000001 - 75012DOC004676
	75013DOC000001 - 75013DOC000810
	75014DOC000001 - 75014DOC000475
	75015DOC000001 - 75015DOC001008
Disk 2	75016DOC000001 - 75016DOC018962
	75018DOC000001 - 75018DOC002993
	75019DOC000001 - 75019DOC004388
	75020DOC000001 - 75020DOC000456
	75021DOC000001 - 75021DOC000117
Disk 3	75017DOC000001 - 75017DOC006388

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Barry W. Graham, Esq.
January 23, 2006
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Disk 4	75022DOC000001 - 75022DOC005830
	75023DOC000001 - 75023DOC001524
	75024DOC000001 - 75024DOC001620
	75025DOC000001 - 75025DOC004839
	75026DOC000001 - 75026DOC000570
	75027DOC000001 - 75027DOC000918
	75028DOC000001 - 75028DOC002237
	75029DOC000001 - 75029DOC006668
	75030DOC000001 - 75030DOC001175
	75031DOC000001 - 75031DOC001769
Disk 5	75034DOC000001 - 75034DOC004583
	75035DOC000001 - 75035DOC005511
	75036DOC000001 - 75036DOC006313
	75037DOC000001 - 75037DOC002225
	75038DOC000001 - 75038DOC006957
	75039DOC000001 - 75039DOC001830
	75040DOC000001 - 75040DOC004427
	75041DOC000001 - 75041DOC001413
	75042DOC000001 - 75042DOC007712
	75043DOC000001 - 75043DOC003223

Very truly yours,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Caryl Arnese
Senior Legal Assistant

Enclosures

Cc: David J. Beck, Esq.

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ERIC FINDLAY

VIA FACSIMILE

February 21, 2006

Edward Naidich
Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
901 New York Avenue, NW
Washington, DC 20001-4413

Re: *BIAX Corp. v. Intel Corp., et al.*
       Case No. 2-05-CV-184-2JW

Dear Ed:

The Montecito code that you requested in your email of February 13, 2006 is now available for your expert's review at our offices in New York.

If you have any questions, please feel free to contact me.

Very truly yours,

Alex V. Chachkes

cc: Harry L. Gillam, Jr., Esq.
       Eric H. Findlay, Esq.
       Eric M. Albritton, Esq.
       B.D. Daniel, Esq.

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May 2, 2006

Alex V. Chachkes, Esq.
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666 Fifth Avenue
New York, New York 10103

VIA E-MAIL &
CONFIRMATION BY MAIL

Re: *BIAX Corp. v. Intel Corp., et al.*
         Case No. 2-05-CV-184-TJW

Dear Alex:

We have completed our initial review of the source code produced by Intel and made available to BIAX's technical expert, Dr. Stone, in electronic form only at your firm's New York offices, for four different processor architectures: Prescott, Merced, McKinley, and Montecito. Now that we have completed our initial review and have revised BIAX's Preliminary Infringement Contentions ("PICs") based on that review, we intend to file a motion with the Court on May 9, 2006, under Patent Rule ("P.R.") 3-7 for leave to amend BIAX's PICs.

Given the newness of the Court's revised P.R.'s with respect to source code claims and refinement of PICs based on production of code and given the circumstances of this case with respect to the claims being asserted and the production of code, we are not certain whether we need to go the P.R. 3-7 route, but we decided it would be the most prudent way to proceed. As explained below, we believe that BIAX has good cause to amend its original PICs. Please let us know by May 8th whether Intel will oppose BIAX's motion. We are attaching copies of the revised claim charts that we intend to file with the Court. We are also attaching a redlined copy of our revised claim charts so that you can see, easily and without having to read the entire document, what specific changes we made.

Our amended PICs assert two new claims against the Montecito version of the Itanium 2: claim 35 of U.S. Patent No. 5,021,945 ("the '945 patent") and claim 24 of U.S. Patent No. 5,517,628 ("the '628 patent"). The addition of these two claims results from the presence of a new feature in the Montecito version of the Itanium 2 processor that Intel refers to as "multi-threading." This multi-threading feature was not present in

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previous versions of the Itanium 2. Because there are no publicly available documents GARRETT &
that describe the Montecito's multi-threading feature, BIAX did not assert claim 35 of the DUNNER LLP
'945 patent or claim 24 of the '628 patent in its initial PICs. However, now that we have
reviewed the Montecito source code, as well as other documents produced by Intel under
P.R. 3-4(a)—all of which was produced by Intel after BIAX's service of its PICs—we
have concluded that these two claims are infringed by the Montecito. Moreover, Intel's
website indicates that Intel has been testing the Montecito version of the Itanium 2 and
thus is currently infringing. Public news reports also indicate that the Montecito is
scheduled for release this summer.

Additionally, we have also made minor revisions for certain elements in claims
asserted in our original PICs to reflect our review of the source code for the Prescott,
Merced, and McKinley architectures. In those places where we have revised the PICs,
we have included citations to the source code to support our infringement position.
Although we do not believe that filing amended PICs are necessary for these previously
asserted claims because the changes are minor, we have included these claims in the
attached charts merely to reflect our review of the source code and to include citations to
the source code where appropriate.

The following tables summarize the two new charts that BIAX has added for the
Montecito version of the Itanium 2 and the changes that BIAX has made to its original
PICs:

New Charts

Patent No.	Accused Product	New Chart
5,021,945	Montecito Version of Itanium 2	Added new chart for claim 35
5,517,628	Montecito Version of Itanium 2	Added new chart for claim 24

Revisions to Original PICs

Patent No.	Accused Product	Changes
4,847,755	Itanium and Itanium 2	minor changes to reflect source code review
4,847,755	Hyper-Threading	minor changes to reflect source code review
5,021,945	Itanium and Itanium 2	minor changes to reflect source code review
5,517,628	Itanium and Itanium 2	no changes
6,253,313	Itanium and Itanium 2	no changes

Moreover, we completed our review of the source code of Intel's four different
architectures as rapidly as possible. The first set of Montecito source code documents
that we received from you were totally garbled due to a printing error. We did not
receive corrected copies of the source code until March 17th. We have worked rapidly
with Dr. Stone to review the source code, which is very complex. At the same time, we
have also been analyzing source code for three different processor architectures of ADI's
products involved in this case.

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We further believe that amending our PICs is consistent with Judge Ward's recognition that "[a]lthough defendants vigorously and rightly guard their source code, until plaintiffs have access to it, plaintiffs are typically unable to give highly specified infringement contentions." Appendix C to the Amended Discovery Order; *see also American Video Graphics, L.P. v. Electronic Arts, Inc.,* 359 F.Supp.2d 558 (E.D. Tex. 2005). This is especially true where Intel has produced very complex source code for four different computer processor architectures and the electronic forms of the code have only been available in your New York offices.

Please let us know whether Intel will oppose BIAX's motion. We agree to Intel's amending its preliminary invalidity contentions based on the revised BIAX PICs within 45 days of the Court's ruling on the motion. We have stamped the enclosed claim charts as "ATTORNEYS' EYES ONLY" because they include citations to Intel's confidential materials.

Sincerely,

Edward Naidich

Encls.

cc: Gil Gillam, Jr., Esq. (via e-mail)
        Eric H. Findlay, Esq. (via e-mail)
        Eric M. Albritton, Esq. (via e-mail)

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GENERAL ORDER 06-6

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

GENERAL ORDER AMENDING PATENT RULE 3-6

It is hereby ORDERED that the following amendment to Appendix M to the local rules, the "Rules of Practice for Patent Cases," having been approved by the judges of this court, is adopted for immediate implementation:[1]

3-6. Final Contentions.

Each party's "Preliminary Infringement Contentions" and "Preliminary Invalidity Contentions" shall be deemed to be that party's final contentions, except as set forth below.

(a) If a party claiming patent infringement believes in good faith that (1) the Court's Claim Construction Ruling or (2) the documents produced pursuant to P. R. 3-4 so requires, not later than 30 days after service by the Court of its Claim Construction Ruling, that party may serve "Final Infringement Contentions" without leave of court that amend its "Preliminary Infringement Contentions" with respect to the information required by Patent R. 3-1(c) and (d).

(b) Not later than 50 days after service by the Court of its Claim Construction Ruling, each party opposing a claim of patent infringement may serve "Final Invalidity Contentions" without leave of court that amend its "Preliminary Invalidity Contentions" with respect to the information required by P. R. 3-3 if:

> (1) a party claiming patent infringement has served "Final Infringement Contentions" pursuant to P. R. 3-6(a), or
>
> (2) the party opposing a claim of patent infringement believes in good faith that the Court's Claim Construction Ruling so requires.

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[1]New language appears in underlined text; deleted language appears in strikeout text.

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Comment: Deletion of the language removes a potential ambiguity from the rule. The former rule language could be read as allowing a party to amend its infringement contentions based on disclosures it received months before so long as the amendment is made within 30 days of receiving the court's *Markman* opinion. Although it makes sense to allow a party to amend its infringement contentions without leave of court based on the *Markman* opinion, a party should not be allowed to wait until after the *Markman* opinion to amend when the amendment is based on disclosures received months before.

The amended rule still allows a party to amend its preliminary infringement contentions within 30 days of the *Markman* without leave of court. Parties also would still be able to amend based on new discovery, but they would need to seek leave (and show good cause) to do so.

Signed this 27 day of February, 2006.

FOR THE COURT:

THAD HEARTFIELD
Chief Judge